AMENDMENTS

Amendments to the Specification:

Please replace paragraph [0038] with the following amended paragraph:

[0038] Figure 5 illustrates one embodiment of a method for packet processing. The framer 240 may be initialized and ready to receive data from the link layer device 250, step 501. Data read request sent on line 453 is generated by the framer engine 350 and sent to the request modifier circuitry 431, step 502. The data read request may be passed to the input FIFO 320 as modified data read request 450 by the request modifier circuitry 431, step 503. Data is sent on line 213 from the link layer device 250 to the input FIFO 320 for protocol processing, step 504. Data modifications are made in the encapsulator engine [[430]] 432, step 505. Data modifications made during this step may include but are not limited to processing the data in multiple stages of a pipeline, packing the data, inserting idle cells, and adding or deleting bytes at the header and/or trailer of the packet. Request modifier circuitry 431 determines if the output FIFO 340 is substantially full by the substantially full signal sent by the output FIFO 340 to the request modifier circuitry 431 on line 454, step 506. If the output FIFO 340 is substantially full then at least one or more of the data read request received on line 453 by the request modifier circuitry 431 may be masked, meaning the request modifier circuitry does not send a modified data read request on line 450 to the input FIFO 320, step 507. The method may continue to mask the data read requests received on line 453 by the request modifier circuitry 431 as long as the output FIFO 340 is substantially full. If the output FIFO 340 is not substantially full then the data read request sent on line 453 may be passed to the input FIFO 320 as modified data read request 450 by the request modifier circuitry 431, step 503. The method may continue to pass the data read requests received on line 453 by the request modifier circuitry 431 as long as the output FIFO 340 is not substantially full.

Please replace paragraph [0047] with the following amended paragraph:

[0052] Figure 7 illustrates another embodiment of a method for packet processing. This method calculates a variation between an input data rate and a pre-determined output data rate. The input data rate may be based on a number of data read requests. The method compensates for the variation by modifying the number of data read requests. In this embodiment, the framer 240 may be initialized and ready to receive data from the link layer device 250 on line 213, and the counter value (count) may be set to zero, step 701. A data read request is generated by the framer engine 350 and transmitted to the request modifier circuitry 631 on line 653, step 702. The data read request may be passed to the input FIFO 320 by request modifier circuitry 631 on line 650, step 703. The data read request may be read by the link layer device 250. In response to a data read request received by the link layer device 250, the link layer device 250 may fetch unpacked data and send it the pre-compute circuitry 633 on line 651 for protocol processing, step [[504]] 704. The link layer device 250 may fetch the data from memory 252. Alternatively, the link layer device 250 may fetch data directly from multiple ports of the physical interface device 290. Pre-compute circuitry 633 calculates the amount of data, total bytes of data, received from the link layer device 250 on line 652 from the input FIFO 320, step 705. The link layer device 250 (e.g., processing device 251 of link layer device 250) may insert additional data or delete data from the input data packets that are transmitted from the link layer device 250 to the physical interface device 260. After calculating the total bytes of data, the pre-compute circuitry 633 may transmit the total bytes of data to the request modifier circuitry 631 on line 660. The request modifier circuitry 631 determines the variation between the input data rate and the pre-determined output data rate. The input data rate is based on the number of data read requests generated by the framer engine 350, and the pre-determined output data rate is based on the pre-determined output data bus width of the physical interface device 260.

The framer engine 350 requests data at a pre-determined output data rate and expects a pre-determined amount of data for every data read request. The variation in bandwidth of packet processing system 200 may be calculated using the total bytes of data received and calculated by pre-compute circuitry 633, and the pre-determined output data bus width expected by the framer engine 350. The request modifier circuitry 631 uses the total bytes of data sent on line 660 to update a counter value, step 706. The current counter value may be updated by subtracting the difference between the total bytes of data and the pre-determined output data bus width from the previous counter value. In alternative embodiments, other methods of updating a counter value may be used.